CHANGXU LIU

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EDUCATION

Wuhan University *HUB, CN*

B.E. in Microelectronics Science and Engineering *Sept. 2018-Jun. 2022*

- Thesis: Research on Fully Homomorphic Encryption Acceleration Methods
- Graduated with Distinction
- GPA: 3.86/4.00

Fudan University *SH, CN*

Ph.D. Candidate in Electronic Science and Technology *Sept. 2022-Jun. 2027 (expected)*

- Supervisor: Prof. Fan Yang.
- Research Interest: Privacy-Preserving Computation Applications; Software-Hardware Co-design
- GPA: 3.37/4.00

PROJECT

Design of Embedded Systems Based on AI Hardware Accelerator *Wuhan University*

Key Project Contributor *Jun. 2020-Sept. 2021*

- Accelerating computationally intensive AI algorithms. Using HLS technology to design a highly parallel convolutional IP.
- Building an embedded system with convolutional IP design for testing in traditional Chinese medicine recognition scenarios.
- Won third place in DIGILENT cup in China Integrated Circuit Innovation and Entrepreneurship Competition 2021.

SoC Design for Zero-Knowledge Proofs *Fudan University*

Key Project Contributor *Apr. 2022-Dec. 2023*

- Responsibility lies in the design of the hard accelerator for the proof generation step of ZKP within the SoC.
- Designing key IPs, including MSM unit and various polynomial processing units
- The MSM accelerator is implemented using the bucket method algorithm, and optimization techniques are applied specifically for parallel computation with multiple PEs. resulting in remarkably high throughput.
- One paper with the first author has been accepted by DAC'24 (CCF-A). One paper with the first author has been accepted by ACM TODAES (CCF-B).

Low Power SoC Design for Large Language Model Inferencing *Fudan University*

Project Leader *May. 2024-Now*

- Responsible for leading the project team, building project document specifications and architectural design of the SoC.
- Design of key IPs in SoCs, Crossbar with native protocols and DMA modules to support parallel data transfers.
- Currently debugging individual modules on FPGA development boards.

PUBLICATIONS

[1] **Changxu Liu**, Danqing Tang, Jie Song, Hao Zhou, Shoumeng Yan, and Fan Yang. 2024. HMNTT: A Highly Efficient MDC-NTT Architecture for Privacy-preserving Applications. In Proceedings of the Great Lakes Symposium on VLSI 2024 (GLSVLSI '24). Association for Computing Machinery, New York, NY, USA, 7–12.

[2] Zhou Hao, **Changxu Liu**, Lan Yang, Li Shang, and Fan Yang. "A Fully Pipelined Reconfigurable Montgomery Modular Multiplier Supporting Variable Bit-Widths".IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2024): 1-1.

[3] **Changxu Liu**, Hao Zhou, Lan Yang, Jiamin Xu, Patrick Dai, and Fan Yang. "Gypsophila: A Scalable and Bandwidth-Optimized Multi-ScalarMultiplication Architecture.". In 2024 61st ACM/IEEE Design Automation Conference (DAC).2024.

[4] **Changxu Liu**, Hao Zhou, Patrick Dai, Li Shang, and Fan Yang. 2024. PriorMSM: An Efficient Acceleration Architecture for Multi-Scalar Multiplication. ACM Trans. Des. Autom. Electron. Syst. 29, 5, Article 77 (September 2024), 26 pages.

[5] Zheng Wu, Jinyi Shen, Xuyang Zhao, **Changxu Liu**, Li Shang and Fan Yang. 2024. TL-CSE: Microarchitecture-Compiler Co-design Space Exploration via Transfer Learning. In 2025 30th Asia and South Pacific Design Automation Conference (ASP-DAC).2025.

[6] Zhou Hao, **Changxu Liu**, Lan Yang, Li Shang, and Fan Yang. "ReZK: A Highly Reconfigurable Accelerator for Zero-Knowledge Proof". IEEE Transactions on Circuits and Systems I: Regular Papers (2024): 1-1.

[7] **Changxu Liu**, Zhou Hao, Lan Yang, Zheng Wu, Patrick Dai, Yinlong Li, Shiyong Wu and Fan Yang. "Myosotis: An Efficiently Pipelined and Parameterized Multi-Scalar Multiplication Architecture via Data Sharing".IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2025): 1-1.

PROFESSIONAL EXPERIENCE

Hardware Engineer Intern, Zhcltech Technology Co., Ltd, Oct. 2021-Apr. 2022 (Mentor: Hanxun Zheng)

Research Intern, Ant Research, Ant Group, Aug. 2023-Feb. 2024 (Mentor: Shoumeng Yan)

HONORS & AWARDS

2021	**First Prize**, China Integrated Circuit Innovation and Entrepreneurship Competition (CICIEC)	*China*
2021	**Meritorious Winner**, Mathematical Contest In Modeling(MCM)	*Online*
2019	**First-class Scholarship**, Wuhan University	*HUB, China*
2019	**First-class Academic Scholarship**, HONGYI Honor College School, Wuhan University	*HUB, China*

SKILLS

English Proficiency	IELTS: 7.5 Listening: 8.5 Reading: 8 Writing: 6.5 Speaking: 6
Programming	Verilog HDL, Python, C++, Scala, MATLAB, LaTeX
Soft Skills	Vivado, VCS, Verdi, Design Compiler, Quartus, Spyglass
Miscellaneous	Linux, Git, AXI protocol