CHANGXU LIU

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EDUCATION

Wuhan University *HB, CN*

B.E. in Microelectronics Science and Engineering *Sept. 2018-Jun. 2022*

- Thesis: Research on Fully Homomorphic Encryption Acceleration Methods
- Graduated with Distinction
- GPA: 3.86/4.00

Fudan University *SH, CN*

Ph.D. student in Electronic Science and Technology *Sept. 2022-Jun. 2027 (expected)*

- Supervisor: Prof. Fan Yang.
- Research Interest: Privacy-Preserving Computation Applications; Software-Hardware Co-design

PROJECT

Design of Embedded Systems Based on AI Hardware Accelerator *Wuhan University*

Key Project Contributor *Jun. 2020-Sept. 2021*

- Accelerating computationally intensive AI algorithms. Using HLS technology to design a highly parallel convolutional IP.
- Building an embedded system with convolutional IP design for testing in traditional Chinese medicine recognition scenarios.
- Won third place in DIGILENT cup in China Integrated Circuit Innovation and Entrepreneurship Competition 2021.

SoC Design for Zero-Knowledge Proofs *Fudan University*

Key Project Contributor *Apr. 2022-Now*

- Responsibility lies in the design of the hard accelerator for the proof generation step of ZKP within the SoC.
- Designing key IPs, including MSM unit and various polynomial processing units
- The MSM accelerator is implemented using the bucket method algorithm, and optimization techniques are applied specifically for parallel computation with multiple PEs. resulting in remarkably high throughput.
- One paper with the first author has been accepted by DAC'24 (CCF-A). One paper with the first author is currently being revised.

PUBLICATIONS

Liu, Changxu, Hao, Zhou, Lan, Yang, Jiamin, Xu, Patrick, Dai, and Fan, Yang. "Gypsophila: A Scalable and Bandwidth-Optimized Multi-ScalarMultiplication Architecture.". In 2024 61st ACM/IEEE Design Automation Conference (DAC).2024.

Liu, Changxu, Danqing, Tang, Jie, Song, Hao, Zhou, Shoumeng, Yan, and Fan, Yang. "HMNTT: A Highly Efficient MDC-NTT Architecture for Privacy-preserving Applications.". In 2024 34th ACM Great Lakes Symposium on VLSI (GLSVLSI).2024.

Zhou, Hao, **Changxu, Liu**, Lan, Yang, Li, Shang, and Fan, Yang. "A Fully Pipelined Reconfigurable Montgomery Modular Multiplier Supporting Variable Bit-Widths".IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2024): 1-1.

PROFESSIONAL EXPERIENCE

 Intern, Zhcltech Technology Co., Ltd, Oct. 2021-Apr. 2022 (Mentor: Hanxun Zheng)

- Hardware Engineer Intern
- Responsible for designing the CSR (Control/Status Register) Ring and a small SoC for the entire AI Accelerator.

 Intern, Ant Group, Oct. Aug. 2023-Feb. 2024 (Mentor: Shoumeng Yan)

- Research Intern
- Investigating circuit optimizations for pipelined NTT and optimizing MDC-type NTT design from a hardware perspective.

HONORS & AWARDS

2021 **First Prize**, China Integrated Circuit Innovation and Entrepreneurship Competition (CICIEC) *China*

2021 **Meritorious Winner**, Mathematical Contest In Modeling(MCM) *Online*

2019 **First-class Scholarship**, Wuhan University *HUB, China*

2019 **First-class Academic Scholarship**, HONGYI Honor College School, Wuhan University *HUB, China*

SKILLS

English Proficiency	IELTS: 7.5 Listening: 8.5 Reading: 8 Writing: 6.5 Speaking: 6
Programming	Verilog HDL, Python (OpenCV, NumPy, Tensorflow. etc.), C++, Scala, MATLAB, LaTeX
Soft Skills	Vivado, VCS, Verdi, Design Compiler, Quartus, Spyglass
Miscellaneous	Linux, Git